# Jose Maria Arnau

## 1. CONTACT INFORMATION


Dr. Jose Maria Arnau

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## 2. EDUCATION

- **UPC BarcelonaTech, March 2011 - April 2015**
  Ph.D. in Computer Architecture
  Grade: Excellent Cum Laude
  Thesis: “Energy-Efficient Mobile GPU Systems”
  Advisers: Prof. Joan-Manuel Parcerisa, Dr. Polychronis Xekalakis
- **UPC BarcelonaTech, October 2010 - September 2011**
  MSc. Degree on Computer Architecture, Networks and Systems
  Grade: 9.75/10 (Award for achieving the highest overall mark)
  Master’s Thesis: “High Performance, Ultra-Low Power Streaming Systems”
  Adviser: Prof. Joan-Manuel Parcerisa
  Co-Advisers: Dr. Polychronis Xekalakis, Prof. Antonio Gonzalez
- **Universitat Jaume I, September 2003 - June 2008**
  BSc. Degree on Computer Engineering
  Grade: 9.64/10 (Award for achieving the highest overall mark)
  Final Year Project: “Development of a Game Engine”
  Adviser: Prof. Miguel Chover Selles

## 3. PROFESSIONAL EXPERIENCE

- **May 2015 - Present: Postdoctoral Researcher, UPC BarcelonaTech**
  I currently hold a postdoctoral research scientist position in the ARCO (Architectures and Compilers) research group. My work investigates energy-efficient architectures for cognitive processors, especially in the areas of automatic speech recognition, object recognition and natural language processing. My research analyzes multiple approaches for achieving high-performance and low-power cognitive computing in mobile devices, including the use of Graphics Processing Units (GPUs), dedicated hardware accelerators and FPGAs. I am currently advising five Ph.D. students.
- **August 2010 - April 2015: Research Assistant, UPC BarcelonaTech**
  I held a research scientist position in the ARCO (Architectures and Compilers) research group, supported by an FI-Research grant from the Catalan Government. I investigated technologies and techniques that improve the energy-efficiency of mobile GPUs, by modifying the driver and the microarchitecture. My Ph.D. analyzed the suitability of decoupled access/execute architectures for mobile graphics hardware to tolerate memory latency in an energy efficient manner. My research also proposed memory bandwidth saving techniques that avoid redundant texture fetches and GPU memoization techniques that remove redundant computations.

- **August 2014 - December 2014: Architecture Intern, NVIDIA Corporation**
  I worked as an intern in the Applied Architecture team at NVIDIA Santa Clara in Silicon Valley. My job consisted on performing GPU power and performance analysis. I also worked on OpenGL compute shader optimization.
- **July 2013 - September 2013: Visiting Researcher, University of Edinburgh**
  I performed a co-design space exploration of compiler optimizations and hardware parameters in GPGPU environments. I used an LLVM-based OpenCL compiler to evaluate the power-performance trade-offs of multiple compiler optimizations, and I explored the hardware design space by using GPGPUSim and GPUWattch.
- **September 2008 - July 2010: Software Developer, Institute of Ceramic Technology**
  I developed several applications for scientific data visualization, using OpenMP for processing massive amounts of data provided by a 3D scanner and OpenGL for rendering 3D tomographies. I also implemented multiple image processing algorithms to automatically detect imperfections in the objects analyzed with the scanner.
- **January 2008 - June 2008: Research Assistant, Universitat Jaume I**
  I developed a game engine for teaching undergraduates with the aim of facilitating the learning of computer graphics. I designed the engine to be simple and clear, but also powerful enough to support visually compelling 3D scenes. I implemented multiple 3D effects, such as per-pixel lighting, dynamic shadows or particle systems, by exploiting modern GPU programmability.

## 3. AWARDS AND HONORS

- **HiPEAC Paper Award** for the publication of "An Ultra Low-Power Hardware Accelerator for Automatic Speech Recognition" in the International Symposium on Microarchitecture (2016).
- **Intel Doctoral Student Honor Programme: $**35000 awarded by Intel Corporation for performing outstanding research in the area of Computer Architecture (2012).
- **FI Research Grant:** funding from the Catalan Government for a three year Ph.D. (2011).
- **Best Student Graduating in Master's Degree on Computer Architecture, Networks and Systems:** awarded by the Barcelona School of Informatics at the UPC BarcelonaTech (2011).
- **Second Best Student Graduating in Computer Engineering in Spain:** awarded by the Spanish Government (2010).
- **Best Student Graduating in Computer Engineering in the Valencian Community:** awarded by the Valencian Government (2009).
- **Best Student Graduating in Computer Engineering:** awarded by the Universitat Jaume I (2008).
- **Best Student Graduating in Computer Engineering:** awarded by the School of Technology and Experimental Sciences of Castellon (2008).
- **Research Collaboration Grant from the Spanish Ministry of Education:** funding for a six month research collaboration in the Computer Graphics Group at the Universitat Jaume I of Castellon (2007).

## 4. PUBLICATIONS

- “UNFOLD: A Memory-Efficient Speech Recognizer Using On-The-Fly WFST Composition”. Reza Yazdani Aminabadi, Jose-Maria Arnau, Antonio Gonzalez. To appear in Proceedings of the IEEE/ACM International Symposium on Microarchitecture (**MICRO**), October 2017.
- "An Ultra Low-Power Hardware Accelerator for Acoustic Scoring in Speech Recognition". Hamid Tabani, Jose-Maria Arnau, Jordi Tubella, Antonio Gonzalez. To appear in Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Sep. 2017.

- "Low-Power Automatic Speech Recognition Through a Mobile GPU and a Viterbi Accelerator". Reza Yazdani, Albert Segura, Jose-Maria Arnau and Antonio Gonzalez. **IEEE Micro**, vol. 37, no. 1, 2017, pp. 22-29.
- "An Ultra Low-Power Hardware Accelerator for Automatic Speech Recognition". Reza Yazdani Aminabadi, Albert Segura, Jose-Maria Arnau, Antonio Gonzalez. In Proceedings of the IEEE/ACM International Symposium on Microarchitecture (**MICRO**), October 2016.
- "Eliminating Redundant Fragment Shader Executions on a Mobile GPU via Hardware Memoization" . Jose-Maria Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis. In Proceedings of the 41st IEEE/ACM International Symposium on Computer Architecture (**ISCA**), June 2014.
- "Parallel Frame Rendering: Trading Responsiveness for Energy on a Mobile GPU" . Jose-Maria Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis . In Proceedings of the 22nd IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**), September 2013.
- "TEAPOT: A Toolset for Evaluating Performance, Power and Image Quality on Mobile Graphics Systems" . Jose-Maria Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis . In Proceedings of the 27th ACM International Conference on Supercomputing (**ICS**), June 2013.
- "Boosting Mobile GPU Performance with a Decoupled Access/Execute Fragment Processor". Jose-Maria Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis . In Proceedings of the 39th IEEE/ACM International Symposium on Computer Architecture (**ISCA**), June 2012.
- "A Decoupled Access/Execute Architecture for Mobile GPUs" . Jose-Maria Arnau, Joan-Manuel Parcerisa and Polychronis Xekalakis . In Proceedings of ACACES, July 2012.
- "Study of the Pressing Operation of Large-sized Tiles Using X-ray Absorption" . J.L. Amoros, G. Mallol, D. Llorens, J. Boix, J.M. Arnau, C.Feliu, J.A. Cerisuelo and J.J. Gargallo. In Proceedings of Qualicer, February 2010.
- "Rapid, Harmless, and Non-destructive Measurement of Ceramic Tile Bulk Density" . G. Mallol, M. Llorens, J. Boix, J.M. Arnau and L. Foucard . In Proceedings of Qualicer, February 2010.

## 5. TEACHING

I am currently co-advising five Ph.D. students along with professor Antonio Gonzalez:

- **September 2015 – Present: Doctoral Advisor**
  Ph.D. Student: Reza Yazdani
  Thesis: Ultra Low-power, High-performance Accelerators for Speech Recognition
- **July 2016 – Present: Doctoral Advisor**
  Ph.D. Student: Albert Segura
  Thesis: Energy-Efficient GPU Architectures for Speech Recognition
- **July 2016 – Present: Doctoral Advisor**
  Ph.D. Student: Marc Riera
  Thesis: Resilient, Low-Power Accelerators for Cognitive Computing
- **September 2016 – Present: Doctoral Advisor**
  Ph.D. Student: Franyell Silfa
  Thesis: Energy-Efficient Architectures for Recurrent Neural Networks
- **September 2016 – Present: Doctoral Advisor**
  Ph.D. Student: Josep-Llorenç Cruz
  Thesis: Reconfigurable Architectures for Automatic Speech Recognition

I am currently advising a student at the Bachelor's Degree on Computer Engineering at UPC:

- **February 2017 – Present: Final Degree Project Advisor**
  BSc. Student: David Ramal Barrios
  Project Title: Implementation of a Neural Network in an FPGA

Past students:

- **September 2015 – June 2016: Master Thesis Advisor**
  Master Student: Albert Segura
  Master's Thesis: Characterization of Speech Recognition Systems on GPU Architectures
  Grade: 9.5/10
  Master in Innovation and Research in Informatics – High Performance Computing
- **February 2016 – June 2016: Final Degree Project Advisor**
  Student: Ferran Olivera
  Project Title: Portability of Speech Recognition Algorithms to an FPGA Platform
  Grade: 10/10
  BSc. Degree on Computer Engineering
- **February 2017 – June 2017: Final Degree Project Advisor**
  Student: Oscar Mañas Sanchez
  Project Title: Adapting Deep Neural Networks to a Low-Power Environment
  Grade: 10/10
  BSc. Degree on Computer Engineering

## 6. TALKS

- "Eliminating Redundant Fragment Shader Executions on a Mobile GPU via Hardware Memoization", International Symposium on Computer Architecture, Minnesota, USA, June 2014.
- "Parallel Frame Rendering: Trading Responsiveness for Energy on a Mobile GPU", International Conference on Parallel Architectures and Compilation Techniques , Edinburgh, UK, September 2013.
- "TEAPOT: A Toolset for Evaluating Performance, Power and Image Quality on Mobile Graphics Systems", International Conference on Supercomputing, Eugene, USA, June 2013.
- "Boosting Mobile GPU Performance with a Decoupled Access/Execute Fragment Processor", International Symposium on Computer Architecture, Portland, USA, June 2012.

## 7. LANGUAGES

- **Spanish:** Native speaker
- **Catalan:** Native speaker
- **English:** Fluent

## 8. OTHER

- Publications Chair of the IEEE/ACM International Symposium on High Performance Computer Architecture (HPCA), Barcelona (Spain), February 2016.
- Participation in research projects:

  - Researcher staff. "Arquitecturas de Sistemas de Computación Inteligentes, Ubicuos y Energéticamente Eficientes". Spanish Ministry of Economy. TIN2016-75344-R. Jan 2017 – Present.

  - Researcher staff. "Microarquitecturas y Compiladores para Futuros Procesadores III". Spanish Ministry of Economy. TIN2013-44375. Jan 2014 – Dec 2016.

  - Researcher staff. "Microarquitecturas y Compiladores para Futuros Procesadores II". Spanish Ministry of Science and Technology, TIN2010-18368, Jan 2011 – Dec 2013.